Conclusions: Two scaled electric models of mesh reflectors have been constructed, and the radiation patterns have been measured. It has been shown that the similarities between the measured and calculated results are very close. The cross-polarisation level is low, and it is very likely that frequency re-use using dual polarisation is indeed possible.

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CMOS LAYOUT DESIGN OF THE HYSTERESIS McCULLOCH–PITTS NEURON

Indexing terms: Networks, Hysteresis

A McCulloch–Pitts neuron is the simplified neuron model which has been successfully used for many optimisation problems. The neural network with the hysteresis property can suppress the oscillatory behaviours of neural dynamics so that the convergence time is shortened. In this paper, digital CMOS layout design of the hysteresis McCulloch–Pitts neuron is presented. Based on simulation results using the hysteresis McCulloch–Pitts binary neuron model, a 6-bit fixed point 2's complement arithmetic was adopted for the calculation of the input U of each neuron. Each neuron needs 204 transistors and requires a $399\lambda \times 368\lambda$ layout area using the MOSIS scalable CMOS/bulk (SCMOS) VLSI technology with $2\mu m$ rule of P well, double level metal. Layout design of the hysteresis McCulloch–Pitts neuron chip was completed, and fabrication of the chip and the design for the test circuit for the fabricated CMOS VLSI chip are underway at present.

Introduction: McCulloch and Pitts proposed a mathematical model of a neuron based on the biological computation in 1943.[1] The input/output function is given by

$$V_i = f(U_i) = \begin{cases} 1 & \text{if } U_i \geq 0 \\ 0 & \text{otherwise} \end{cases} \quad (1)$$

where V_i and U_i are the output and the input of the ith neuron, respectively. The McCulloch–Pitts neuron and the modified McCulloch–Pitts neuron have been successfully used for graph planarisation problems,[2] tiling problems,[3] RNA secondary structure prediction problems,[4,5] maximum independent set problems,[5] sorting problems,[6] and k-colourability problems.[7]

The McCulloch–Pitts neural network is shown to converge faster than the sigmoid neural network.[8] The sigmoid neural network introduced by Hopfield and Tank in 1985[9] is composed of sigmoid neurons, where the relation between output V_i and input U_i for the ith neuron is given by

$$g(U_i) = \frac{1}{2}\left[1 + \tanh\left(\frac{U_i}{U_0}\right)\right] \quad (2)$$

In eqn. 2, U_0 is a constant called gain. However, the CMOS neural network introduces undesirable oscillatory behaviour. To overcome this problem, we introduced a hysteresis McCulloch–Pitts binary neuron model, discussed in Reference 10. The hysteresis property suppresses the oscillatory behaviour of neural dynamics so that the convergence time is consequently shorter. The hysteresis McCulloch–Pitts binary neuron has been successfully used for crossbar switch scheduling[10] and fault-cell allocation.[11] Fig. 1 shows the input/output relation of the hysteresis McCulloch–Pitts binary neuron model. The output of the ith hysteresis McCulloch–Pitts binary neuron V_i is given by

$$V_i = \begin{cases} 1 & \text{if } U_i \geq \text{UTP (upper trip point)} \\ 0 & \text{if } U_i \leq \text{LTP (lower trip point)} \\ \text{unchanged} & \text{if LTP} < U_i < \text{UTP} \end{cases} \quad (2)$$

where U_i is the input of the ith neuron. The output at any moment depends upon the present value of the input and the past values of the output.

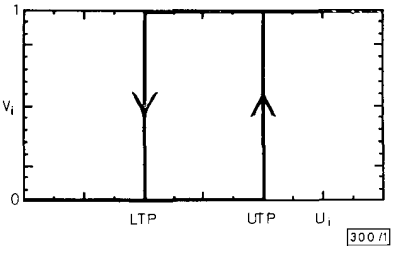

Fig. 1 *Hysteresis binary function*

Layout design of the hysteresis McCulloch–Pitts binary neuron: There have been many investigators implementing the sigmoid and binary neurons. However, there is no implementation of the hysteresis McCulloch–Pitts binary neuron. There are two kinds of implementation methods for neural networks: digital circuits and analogue circuits. It is easier to implement neural networks using digital circuits than using analogue circuits because the digital approach is more tolerant of unavoidable variations.[12] Furthermore, the CMOS digital VLSI technology is one of the most successful technologies today. Thus, we present VLSI layout design of the hysteresis McCulloch–Pitts binary neuron using the CMOS digital VLSI technology.

Our simulation results[2–7] using the hysteresis McCulloch–Pitts binary neuron model give the following facts:

(1) The computation resolution with the range from -15 to 10 in integer numbers is sufficient for the correct motion of each neuron. (2) The maximum hysteresis range is 10. If the hysteresis range is too big, the convergence speed of the system is found to be very low. Based on these facts, we set the following architecture for CMOS VLSI design of the hysteresis McCulloch–Pitts binary neurons:

(i) To realise the hysteresis property, we design a sequential circuit using flip-flop programming.

(ii) The fixed point 2's complement arithmetic is used for calculation of U which requires additions and subtractions only.

(iii) To express the value of U, we use 6 bits with 2's complement arithmetic which is sufficient to express the integer range from -15 to 10.

(iv) For simplicity, the LTP is set at 0 and the UTP can be reset between 0 and 7. Thus, the maximum hysteresis range can be expressed with 3 bits.

Fig. 2 shows the state transition of the hysteresis McCulloch–Pitts binary neuron. Here, two circles represent two different states, where the output of the neuron is 0 or 1, respectively. Each arrow indicates the state transition. The numbers attached to each arrow represent the range of the input.

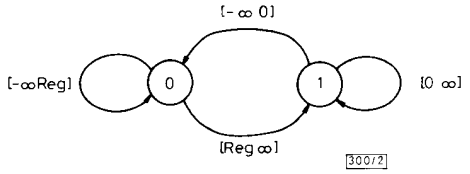

Fig. 2 *State transition of hysteresis McCulloch–Pitts binary neuron*

Fig. 3 shows the digital circuit diagram of the hysteresis McCulloch–Pitts binary neuron. The 5-bit input $U(U0, U1, \ldots, U5)$ is compared at the 5-bit comparator with the specific value which will be equal to either LTP or UTP. A multiplexer realised by three NOR gates transmits the value of LTP or the value of UTP according to the previous state of the neuron itself which is labelled as 'V' and is stored in a leftmost flip-flop in Fig. 3. The state of a neuron is updated synchronously with a clock signal labelled 'CK2'. The 3-bit value of UTP is stored in the 3-bit shift register through the serial input line named 'Hys'. For this purpose, another clock signal labelled 'CK1' is used. To initialise the whole circuit, a line named 'CLR' is prepared. This line is connected with a reset circuit including the power-on reset circuit and the manual reset circuit which is fabricated out of the VLSI chip.

The proposed circuit of the hysteresis McCulloch–Pitts binary neuron using the CMOS VLSI technology is simulated using a logic simulator on a Macintosh SE/30. Fig. 4*a* shows the timing diagram of our simulation result. At the beginning of our simulation, one negative pulse is given to CLR to reset the flip-flops for the initial state. After three clock cycles of CK1, the 3-bit value as the maximum hysteresis range is loaded into the 3-bit shift register. To simulate the hysteresis function, twelve state changes (each state is denoted by *A*, *B*, ..., *M* in Fig. 4*b*) are given to the circuit. The correct motion

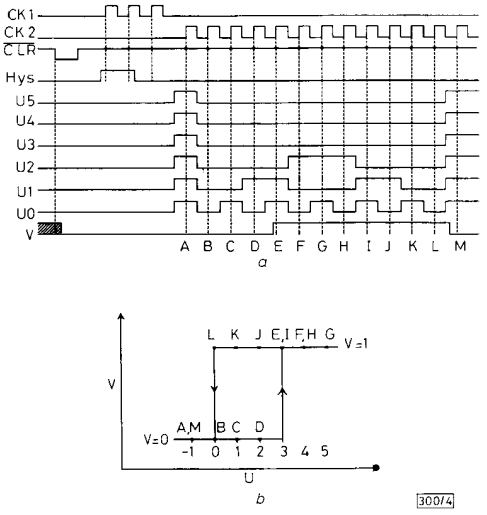

Fig. 4 *Simulation result of hysteresis McCulloch–Pitts binary neuron*
a Timing diagram of the simulation result
b Thirteen states of the simulated points

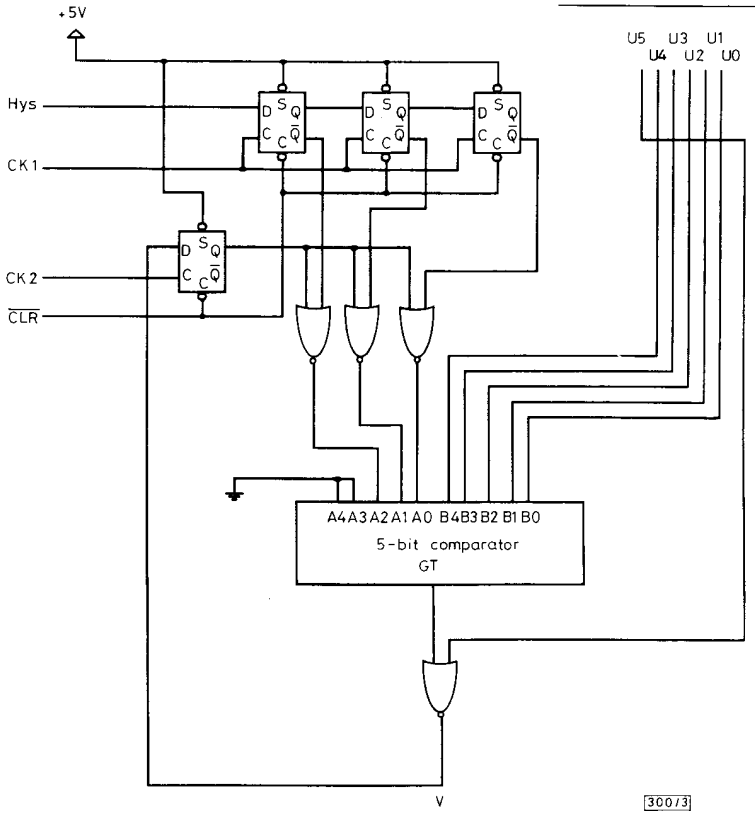

Fig. 3 *Digital circuit diagram of hysteresis McCulloch–Pitts binary neuron*

of the output V of the hysteresis McCulloch–Pitts binary neuron is confirmed.

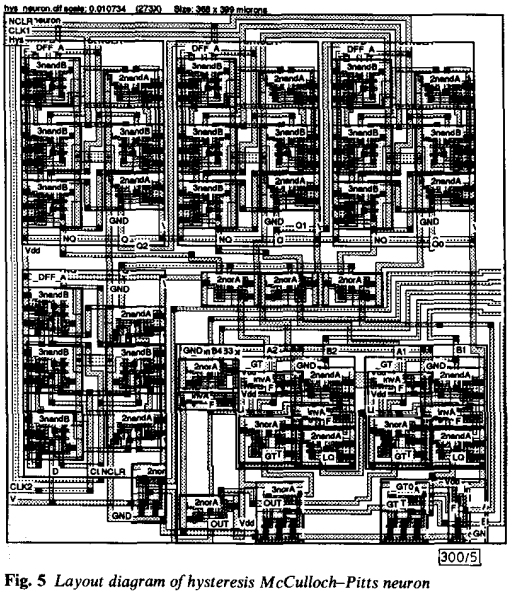

Fig. 5 *Layout diagram of hysteresis McCulloch–Pitts neuron*

Fig. 5 shows the layout diagram of a hysteresis McCulloch–Pitts binary neuron using the MOSIS scalable CMOS/bulk (SCMOS) VLSI technology with 2 μm rule of P well, double level metal. Each neuron needs a $399\lambda \times 368\lambda$ layout area using the MOSIS scalable CMOS/bulk (SCMOS) VLSI technology with 2 μm rule of P well, double level metal. Layout design of the hysteresis McCulloch–Pitts binary neuron chip was completed. We are fabricating the chip and designing the test circuit for the fabricated CMOS VLSI chip at present.

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CW OPERATION OF SEMICONDUCTOR RING LASERS

Indexing terms: Semiconductor lasers, Lasers

Semiconductor ring lasers have been fabricated in single quantum well material using electron-beam lithography and $SiCl_4$ dry etching. CW operation has been achieved in 84 μm diameter rings at a threshold current of 24 mA. This low value makes the structure very suitable for monolithic integration in optoelectronic circuits.

Introduction: The vast majority of semiconductor lasers rely on a Fabry–Perot cavity formed by two cleaved facets which are very easily fabricated. However, when the laser is to be integrated monolithically with other optical or electronic components, the need for cleaved facets constitutes a severe constraint, so that alternative methods of providing feedback are required. The following methods have been reported concerning a Fabry–Perot cavity:

(1) A grating as a distributed feedback element in DFB and DBR lasers overcomes the need for one or both cleaved facets. Such lasers, however, are difficult to fabricate and the structure requires overgrowth.

(2) Dry etching has been demonstrated[1] as a suitable technique for fabricating facets nearly as smooth as cleaved ones. The use of a faceted laser in an optoelectronic integrated circuit (OEIC), however, introduces additional losses when coupling into subsequent components of the system.

(3) Microcleaving[2] has the further disadvantage of requiring very high mesas, which is very undesirable for multilevel lithography.

An alternative to those different techniques of forming a Fabry–Perot cavity is to use a circular waveguide resonator, an approach which completely eliminates the need for a facet. The few attempts of such devices with reported threshold currents of 300 mA,[3] 180 mA[4] and 80 mA[5] demonstrated the potential of the structure, but the threshold currents were still too high for practical devices. Other authors[6,7] have reported on semi- or quartercircle structures, but those do require one or two cleavings which is unacceptable for complex integration.

In this letter we report the first CW operation of semiconductor ring lasers to our knowledge.

Design: The structure that was fabricated is a pillbox (Fig. 1), where the effect of the 'whispering gallery'[8] is used as a guiding mechanism. The whispering gallery modes undergo total internal reflections at the outer GaAs–air interface without requiring an inner boundary providing the angle of incidence is shallow. A different approach to understanding the guiding mechanism has been previously reported[5] by transforming the curved structure into a straight one using the conformal transformation technique.[9] As a result, the refractive index within the transformed guide is represented by the following dependence on the radius:

$$n(r) = n(\rho)e^{r/R}$$

with $n(\rho)$ being the initial index distribution and R the radius of the structure that has been transformed. This expression illustrates that the transformed refractive index increases